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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/941,537
Filing Date: August 29, 2001
Appellant(s): CHEN ET AL.

Randy W. Tung
For Appellant

EXAMINER'S ANSWER

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This is in response to the appeal brief filed October 15, 2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences, which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The Appellants' statement of the status of amendments after final rejection contained in the brief is incorrect, at least because (a) the brief unnecessarily includes the status of an amendment filed on August 1, 2003, before the final rejection mailed on September 11, 2003 and (b) the brief seems to confuse the date when the final rejection was mailed (September 11, 2003) with the date when the first after final amendment was actually filed (November 10, 2003). A simplified listing showing only the date and correct status of each after final amendment is as follows:

The amendment (after final rejection) filed on November 10, 2003 has not been entered.

The amendment (after final rejection) filed on December 15, 2003 has not been entered.

The amendment (after final rejection) filed on February 11, 2004 has not been entered.

The amendment (after final rejection) filed on May 4, 2004 has not been entered.

The amendment (after final rejection) filed on July 21, 2004 **has been entered.**

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The Appellants' statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellants' brief includes a statement that the claims do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6,042,999	Lin et al.	3-2000
6,027,861	Yu et al.	2-2000
5,918,147	Filipiak et al.	6-1999

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 7-8, 10-11, 13-15, and 17-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US Patent 6,042,999) in view of Yu et al. (US Patent 6,027,861), and further in view of Filipiak et al. (US Patent 5,918,147).

Lin teaches a robust dual damascene photolithographic process with reduced light reflectance. The process starts by providing a semiconductor substrate having substructure devices formed in or on the substrate, including metal layers (column 4, lines 35-54). A lower layer dielectric (LLD) 110 (pointed out as an intermetal dielectric, IMD, when coated on metal, column 4 lines 57-61), a thin conformal etch-stop layer 120, and an upper layer dielectric (ULD) 130 are formed on the substrate (instant claim 2). Both lower and upper dielectric (LLD and ULD) layers may be formed of silicon oxynitride (SiON, SiO_xN_y), silicon nitride (Si_3N_4, SiN), or silicon oxide by PECVD, CVD, PVD, or sputtering, preferably to a thickness of 8,000 to 15,000 Angstroms (Å) (column 5 lines 1-9, instant claims 21-22). The etch-stop layer can be silicon oxynitride (SiON, SiO_xN_y), silicon nitride (Si_3N_4, SiN), or titanium nitride (TiN) (e.g., to a thickness of 500-1,500 Å, etc., column 5 lines 10-20, instant claim 3). These layers are followed

by forming and patterning a photoresist 145 having an opening 145′, as shown in Figure 2a and described at column 4 line 55 to column 5 line 24. Even though described and shown in terms of a single via opening and overlapping trench, column 1 lines 22-31 clearly state the intention of forming plural grooves or trenches and conductive holes or via openings to form plural multi-level interconnects by repeating the dual damascene process as many times as is required. This encompasses formation of plural substantially adjacent via openings (instant claims 10 and 18). A via opening 145 is etched through both dielectric layers and the intervening etch-stop layer (e.g., of ARC material, etc.) down to the substrate using the photoresist as an etching mask, then the photoresist is removed by oxygen ashing as shown in Figure 2b (column 5 lines 24-34). A main feature and key aspect of this process includes formation of an anti-reflectance coating (e.g., ARC, bottom ARC (BARC), etc.) 150 as a protective cover over the dielectric (e.g., IMD, etc.) upper surface and in the via opening 145, covering the via sidewalls and bottom to the point of filling the via opening; then forming and patterning another photoresist layer 160 with an opening or trench 165′ over the via opening as shown in Figure 2c. Suitable ARC materials include titanium nitride (TiN), silicon oxynitride (SiON), and/or organic materials (column 5 lines 35-61, instant claims 7 and 23-24). This ARC or BARC 150 can be either opaque or translucent, and yet not reflect electromagnetic radiation. These ARC properties hint at the usefulness of a second underlying ARC (instant claims 11, 13-15, and 19-20). While not specifying an alternative embodiment requiring non-filling of the ARC layer in the holes or openings, it is readily apparent that adequate protection could also be obtained by using one or more ARC layers of sufficient thickness without necessarily requiring that the ARC material fill one or more via openings or holes, provided that the openings or holes have widths of more than

twice a total sufficient ARC layer thickness on the sidewalls of the openings or holes. In fact, prior art Figures 1c-1f show just such a configuration for a thin conformal etch barrier layer or an etch stop layer 50, which is coated on the sidewalls of an opening or hole without filling the opening or hole and is conventionally formed of silicon oxynitride (SiON, SiO_xN_y), silicon nitride (Si_3N_4, SiN) and/or titanium nitride (TiN) (column 2, lines 4-64). These same materials have already been noted above for their utility as ARC layers, so these etch stop materials are also expected to inherently function as ARC layers about 500-1,500 Å thick (instant claims 1, 3, 8, and 17 for an ARC thickness of 100-1,000 Å).

While teaching at least portions of most of the limitations found in claims 1-3, 7-8, 10-11, 13-15, and 17-24 as pointed out above (even though some of these limitations were interpreted as inherent in the cited reference), Lin does not directly teach limiting the ARC layer thickness to about 100-1,000 Å on the sidewalls of the via openings or holes without filling the openings or holes and does not specify using plural overlapping ARC layers (though the usefulness of such a combination is hinted by stating that the ARC can be translucent).

Yu shows suitability of a TiN barrier layer (18, 46) as a thin conformal ARC layer (about 200-1,500 Å thick, shown as 18 in Figures 4-6 and as 46 in Figures 8-12) in reducing undesirable back scattering of light during patterning of an overlying photoresist for subsequent etching therethrough to form via openings for metal interconnects in semiconductor fabrication (column 4 lines 33-62 and column 5 lines 27-41).

Filipiak discloses tailoring plural ARC (e.g., silicon nitride, silicon-rich silicon nitride, silicon oxynitride, titanium nitride, etc.) layer combinations to their intended placement in a semiconductor device to avoid reflective notching when patterning an overlying photoresist layer

(column 1 lines 11-20). Plural layer antireflective coatings (ARC) disclosed as suitable for semiconductor device manufacture include ARC 38 in Figure 5 which is composed of portions 380, 382, and 384 (column 3 lines 20-27) and conformal ARC 86 in Figure 10 which is composed of portions 861, 862, and 863 (column 4 lines 36-51). As shown in Figure 6 and described at column 3 lines 48-55, ARC portions 380, 382, and 384 are 50, 100 and 200 Å thick, respectively, and are typically only as thick as needed to serve their intended purpose.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the dual damascene photolithographic process for reducing light reflectance taught by Lin as discussed above with additional conformal antireflective coating (ARC) layer(s) 50-1,500 Å thick as shown by Yu and disclosed by Filipiak, which fully encompasses instant claims 8 and 17 for ARC(s) 100-1,000 Å thick. It would also have been obvious to apply at least one thin conformal ARC layer to the sidewalls of the holes or openings without filling the holes or openings before patterning an overlying photoresist layer to avoid reflective notching of the photoresist, as taught by Lin and disclosed by Filipiak. Both of these are because all these references relate to the same art of semiconductor device manufacture for the purpose of reducing undesirable reflectance by using one or more ARC layer(s) to avoid reflective notching of an overlying photoresist layer during patterning.

(11) Response to Arguments

Issue 1: Whether or not claims 1-3, 21, and 23 are unpatentable over Lin et al. (US Patent 6,042,999) in view of Yu et al. (US Patent 6,027,861), and further in view of Filipiak et al. (US Patent 5,918,147).

On pages 9-10 of their appeal brief, Appellants state that Lin teaches a dual damascene process that involves filling a via opening with protective material prior to patterning an overlying trench (abstract). Appellants admit that Lin's protective material is disclosed to be a BARC layer (e.g., silicon oxynitride, organic material, etc.) that fills the via opening (column 5 lines 35-57, Figure 2C), but argue that a portion of the BARC layer is removed from the filled via opening to about a level of an intervening etch stop layer. Appellants further state that Lin's BARC protective layer is etched back either before or along with etching of the overlying trench (column 5 lines 1-14 and 57-65).

Appellants argue on page 11 that Lin teaches filling the via opening with an ARC material, thereby requiring subsequent etchback to remove the ARC filling prior to trench patterning to protect the bottom of the via opening (column 6 lines 7-14). Appellants further argue on page 11 that impermissible hindsight reasoning was used in regard to Lin alone and argue on page 12 that neither Yu nor Filipiak cure the deficiencies of Lin to establish a prima facie case of obviousness against the instant claims. Appellants also assert on page 13 that there is no apparent motivation or suggestion for combining the teachings of Yu with those of Lin.

In response to Appellants' arguments on page 11 against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In response to Appellants' argument on page 11 that the Examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight

reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). Lin points out that in a dual damascene process it is conventionally known to use a thin conformal etch barrier layer 50 of about 1,000 Å thick to cover the sidewalls of a hole through insulating layers, without filling the hole (see prior art Figures 1c-1f). Conventional etch barrier layer materials include silicon oxynitride (SiON, SiO_xN_y), silicon nitride (Si_3N_4, SiN) and/or titanium nitride (TiN) (column 2, lines 4-64). These same materials have also been shown useful for ARC layers, as noted above. In addition, Yu and Filipiak expand this range for ARC layer thickness to 50-1,500 Å, as previously explained. This establishes that coating (via) opening sidewalls with an ARC or etch barrier layer without filling the opening was within the level of ordinary skill at the time the invention was made. In fact, Filipiak teaches that an ARC layer is typically only as thick as needed, which suggests that ARC material could be saved and subsequent removal could even be avoided by keeping the ARC layer(s) as thin as possible, while still preventing undesirable back scattering of light that leads to reflective notching of an overlying resist during patterning.

In response to Appellants' argument on page 13 that there is no apparent motivation or suggestion for combining the teachings of Yu with those of Lin, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ

871 (CCPA 1981). Both Lin and Yu address the suitability of a thin conformal ARC layer of the same or similar material in reducing undesirable back scattering of light during patterning of an overlying photoresist during semiconductor fabrication. Additionally, it is noted that the term "conformal" indicates that the protective ARC layer conforms to a shape, profile, or surface configuration similar to that of the substrate before coating. Therefore, applying a thin conformal protective ARC layer on an underlying surface would include coating of hole or opening sidewalls without filling the hole or opening, as recited in the instant claims. The reason for combining Filipiak with Lin and Yu is to tailor plural ARC layers of the same or similar material as those used in Lin and/or Yu in semiconductor device fabrication to avoid reflective notching when patterning an overlying photoresist layer. Filipiak further bolsters the use of thin conformal ARC layers by stating that they are typically only as thick as needed. This would be expected to overcome the need for subsequent removal of an ARC filling from the via opening either before or during etching of an overlying trench in Lin's dual damascene process. Filipiak describes one alternative single layer ARC, called "the antireflective layer", as typically having a thickness of 100-1,000 Å and often having a thickness of 200-500 Å (column 2, lines 58-60). Further, Filipiak teaches that using a continuously graded material composition as an alternative to using plural separate ARC layers of different material, such as described at column 3 lines 12-30, can enhance compatibility of a single ARC layer. As stated above, Filipiak also addresses the utility of plural compatible ARC layers, which are tailored to maintain compatibility with a particular utility while still serving to avoid reflective notching when patterning an overlying photoresist layer.

In response to Appellants' argument on pages 13-14 that there is no suggestion to combine the references, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the reasons for combining Yu and Filipiak with Lin have been set forth above. All three references relate to the same art of semiconductor device manufacture for the purpose of reducing undesirable reflectance by using one or more ARC layer(s) to avoid reflective notching of an overlying photoresist layer during patterning. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the dual damascene photolithographic process for reducing light reflectance taught by Lin as discussed above with additional conformal antireflective coating (ARC) layer(s) 50-1,500 Å thick as shown by Yu and disclosed by Filipiak, which fully encompasses the instant claims for ARC(s) 100-1,000 Å thick. It would also have been obvious to apply at least one thin conformal ARC layer to the sidewalls of the holes or openings without filling the holes or openings before patterning an overlying photoresist layer to avoid reflective notching of the photoresist, as taught by Lin, Yu, and Filipiak. The reason for combining Filipiak with Lin and Yu is to tailor plural ARC layers of the same or similar material as those used in Lin and/or Yu for semiconductor device fabrication to avoid reflective notching when patterning an overlying photoresist layer. Filipiak further bolsters the use of thin conformal ARC layers by stating that they are typically only as thick as needed. This would be expected to overcome the need for

subsequent removal of an ARC filling from the via opening either before or during etching of an overlying trench in Lin's dual damascene process.

Issue 2: Whether or not claims 7 and 8 are unpatentable over Lin et al. (US Patent 6,042,999) in view of Yu et al. (US Patent 6,027,861), and further in view of Filipiak et al. (US Patent 5,918,147).

On page 15, Appellants reiterate their previous statements with respect to Issue 1. Responses to these statements have already been set forth above.

With respect to claim 7, Appellants assert on page 15 that the instant invention does not disclose or claim a Ti/TiN hardmask layer, which also functions as an ARC as disclosed by Yu, but rather the instant invention discloses a TiN ARC as one element of a Markush group for forming an ARC according to claim 1. However, Yu also shows the suitability of a TiN barrier or hardmask layer (18 in Figures 4-6 and 46 in Figures 8-12) as a thin conformal ARC layer (about 200-1,500 Å thick) in reducing undesirable back scattering of light during patterning of an overlying photoresist for subsequent etching therethrough to form via openings for metal interconnects in semiconductor fabrication (column 4 lines 33-62 and column 5 lines 27-41). This use of a thin conformal TiN ARC as taught by Yu has been maintained throughout the prosecution of this application and has not been disputed by Appellants. Therefore, Appellants' most recent assertion regarding Yu's Ti/TiN hardmask/ARC layer is immaterial and does not overcome the outstanding obviousness rejection over the combination of Lin, Yu, and Filipiak, for at least the reasons previously established.

Appellants also argue on pages 15-16 that no support was provided for expecting the etch stop material shown in Lin's prior art Figures 1c-1f to have the inherent functionality of an ARC. Appellants further argue that Lin only discloses the use of SiN as an etch stop material (see the sentence bridging pages 15 and 16), but further stipulate on page 16 that SiON is also well known as having antireflectance properties (for use as an ARC, page 16).

Appellants appear to be mistaken about the teachings of Lin. At column 2 lines 34-41, Lin clearly teaches that conventional etch barrier or etch stop material 50 (as shown in Figure 1c) includes silicon oxynitride (SiO_xN_y, which includes SiON) and titanium nitride (TiN) alternatives, as well as silicon nitride (Si_3N_4, SiN). At column 5 lines 10-20, Lin describes forming an etch-stop layer that is alternatively silicon oxynitride (SiON, SiO_xN_y), silicon nitride (Si_3N_4, SiN), or titanium nitride (TiN) (e.g., to a thickness of 500-1,500 Å, etc.). Lin further teaches that suitable ARC materials include titanium nitride (TiN), silicon oxynitride (SiON), and/or organic materials (column 5 lines 35-61). Thus, Lin identified at least two materials (titanium nitride (TiN) and silicon oxynitride (SiON)) as being suitable for either etch stop layers or ARCs. The same material can readily be expected by one of ordinary skill in the art to inherently possess the same properties, absent convincing evidence to the contrary. See MPEP 2112 [R-2]. See also In re Papesch, 315 F.2d 381, 391, 137 USPQ 43, 51 (CCPA 1963) ("From the standpoint of patent law, a compound and all its properties are inseparable.") (MPEP 2141.02). Therefore, either titanium nitride (TiN) or silicon oxynitride (SiON) etch stop layers would have been expected to also inherently function as ARCs at the time the invention was made.

Appellants argue on pages 16-17 that the prior art disclosed by Lin at column 2 lines 34-52 refers to a totally different process of manufacturing dual damascenes that requires depositing an etch barrier layer into a trench opening (along the sidewalls thereof without filling the trench), then etching a via hole through the bottom of the trench. Appellants further argue on pages 17-18 that this method of Lin's prior art would not work either in Appellants' instant claimed process or in Lin's teaching of either a separate or simultaneous etching step to remove a portion of a protective (ARC) material during etching of an overlying trench. Appellants also contend on pages 17-18 that Lin's principle of operation is completely different from that of Appellants' claimed invention.

In response to Appellants' arguments on pages 16-18 against the reference (Lin) individually, one cannot show nonobviousness by attacking a reference individually where the rejection is based on a combination of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants are again reminded that the outstanding obviousness rejection of the instant claims under 35 USC 103 is not based on Lin alone, but rather on Lin in combination with Yu and Filipiak, for the reasons previously given.

In response to Appellants' arguments on pages 16-18 that there is no apparent motivation or suggestion for combining the teachings of Yu and Filipiak with those of Lin (including Lin's disclosed prior art), the test for obviousness is not whether the features of a secondary reference (such as those shown in Lin's prior art) may be bodily incorporated into the structure of the primary reference (such as those shown by the dual damascene process taught by Lin as discussed above); nor is it that the claimed invention must be expressly suggested in any one or

all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). Both Lin and Yu address the suitability of a thin conformal ARC layer of the same or similar material in reducing undesirable back scattering of light during patterning of an overlying photoresist during semiconductor fabrication. Additionally, it is noted that the term "conformal" indicates that the protective ARC layer conforms to a shape, profile, or surface configuration similar to that of the substrate before coating. Therefore, applying a thin conformal protective ARC layer on an underlying surface would include coating of hole or opening sidewalls without filling the hole or opening (whether a via opening or a trench opening), as recited in the instant claims. The reason for combining Filipiak with Lin and Yu is to tailor plural ARC layers of the same or similar material as those used in Lin and/or Yu in semiconductor device fabrication to avoid reflective notching when patterning an overlying photoresist layer. Filipiak further bolsters the use of thin conformal ARC layers by stating that they are typically only as thick as needed. This would be expected to overcome the need for subsequent removal of an ARC filling from the via opening either before or during etching of an overlying trench in Lin's dual damascene process. Filipiak describes one alternative single layer ARC, called "the antireflective layer", as typically having a thickness of 100-1,000 Å and often having a thickness of 200-500 Å (column 2, lines 58-60). Further, Filipiak teaches that using a continuously graded material composition as an alternative to using plural separate ARC layers of different material, such as described at column 3 lines 12-30, can enhance compatibility of a single ARC layer. As stated above, Filipiak also addresses the utility of plural compatible ARC

layers, which are tailored to maintain compatibility with a particular utility while still serving to avoid reflective notching when patterning an overlying photoresist layer.

In regard to Appellants' contention on pages 17-18 that Lin's principle of operation is completely different from that of Appellants' claimed invention, it is noted that Appellants do not further elaborate their specific reason(s) for this contention. Therefore, it is not certain whether Appellants are comparing their claimed invention to (a) Lin's disclosed prior art process of manufacturing dual damascenes that requires depositing an etch barrier layer into a trench opening (along the sidewalls thereof without filling the trench), then etching a via hole through the bottom of the trench (understood to be a trench-then-via process) or (b) Lin's teaching of either a separate or simultaneous etching step to remove a portion of a protective (ARC) material (in a previously formed via) during etching of an overlying trench (understood to be a via-then-trench process).

Since the instant claims read on a via-then-trench process as taught by Lin in view of Yu and Filipiak, this was the main reason for citing Lin as the primary reference (in accordance with (b) above). In response to comparison (b) above, the reason for combining Yu and Filipiak with Lin is to tailor plural ARC layers of the same or similar material as those used in Lin and/or Yu in semiconductor device fabrication to avoid reflective notching when patterning an overlying photoresist layer. Filipiak further bolsters the use of thin conformal ARC layers by stating that they are typically only as thick as needed. This would be expected to overcome the need for subsequent removal of an ARC filling from the via opening either before or during etching of an overlying trench in Lin's dual damascene process. Filipiak describes one alternative single layer ARC, called "the antireflective layer", as typically having a thickness of 100-1,000 Å and often

having a thickness of 200-500 Å (column 2, lines 58-60). Further, Filipiak teaches that using a continuously graded material composition as an alternative to using plural separate ARC layers of different material, such as described at column 3 lines 12-30, can enhance compatibility of a single ARC layer. As stated above, Filipiak also addresses the utility of plural compatible ARC layers, which are tailored to maintain compatibility with a particular utility while still serving to avoid reflective notching when patterning an overlying photoresist layer. This combination of references is not believed to require changing the basic principle of operation for Lin's via-then-trench dual damascene process, at least because the combined process is still a similar via-then-trench process that involves forming thin conformal ARC layers on the sidewalls of at least one via opening without filling the at least one via opening.

In response to comparison (a) above, Lin's disclosed prior art trench-then-via dual damascene process (as shown in Lin's Figures 1c-1f) was not intended for direct comparison with Appellants' instant claimed process or even to be bodily incorporated into the overall combination of Lin, Yu, and Filipiak. Rather, this prior art trench-then-via dual damascene process disclosed by Lin was cited to show the usefulness and practicality of forming a thin conformal layer (on sidewalls of an opening without filling the opening) of conventional etch barrier or etch stop material that includes silicon oxynitride (SiO_xN_y, which includes SiON) and titanium nitride (TiN) alternatives, as well as silicon nitride (Si_3N_4, SiN). At column 5 lines 10-20, Lin describes forming an etch stop layer that is alternatively silicon oxynitride (SiON, SiO_xN_y), silicon nitride (Si_3N_4, SiN), or titanium nitride (TiN) (e.g., to a thickness of 500-1,500 Å, etc.). Lin further teaches that suitable ARC materials include titanium nitride (TiN), silicon oxynitride (SiON), and/or organic materials (column 5 lines 35-61). Therefore, it would have

been obvious to one of ordinary skill in the art at the time the invention was made to have reduced the thickness of the ARC as suggested by Yu and Filipiak in Lin's via-then-trench dual damascene process so that the ARC was no thicker than needed, as taught by Filipiak.

Issue 3: Whether or not claim 10 is unpatentable over Lin et al. (US Patent 6,042,999) in view of Yu et al. (US Patent 6,027,861), and further in view of Filipiak et al. (US Patent 5,918,147).

On page 19, Appellants reiterate their previous statements with respect to Issues 1 and 2. Responses to these statements have already been set forth above.

Appellants argue on pages 19-20 that neither Lin, Yu, nor Filipiak teach or disclose forming at least two via openings "substantially adjacent to one another" in a dual damascene process.

Since the instant claims, even when read in light of the disclosure, do not give any dimensions that specifically limit the distance between two via openings that are "substantially adjacent to one another", this phrase was given it's broadest reasonable interpretation. This broadest reasonable interpretation includes any two via openings in or on the same substrate (of a semiconductor device). Even though Lin's teachings are described and shown in terms of a single via opening and overlapping trench, Lin's column 1 lines 22-31 clearly state the intention of forming plural grooves or trenches and conductive holes or via openings to form plural multi-level interconnects by repeating the dual damascene process as many times as is required. This encompasses the formation of plural (at least two) via openings that are "substantially adjacent to one another". However, Appellants are reminded that even if the combination of references

(Lin, Yu, and Filipiak) fail to show a certain feature of Appellants' disclosed invention, it is noted that the feature upon which Appellants rely (i.e., "especially where metal interconnect lines are in a head-to-head design" in reference to the proximity of substantially adjacent via openings) is not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Issue 4: Whether or not claims 11, 13-14, 19, and 22 are unpatentable over Lin et al. (US Patent 6,042,999) in view of Yu et al. (US Patent 6,027,861), and further in view of Filipiak et al. (US Patent 5,918,147).

On page 20, Appellants reiterate their previous statements with respect to Issues 1-3. Responses to these statements have already been set forth above.

Appellants argue on pages 20-21 that none of the cited references suggest or disclose the following steps recited by Appellants' claim 11: [1] providing a first anti-reflectance coating (ARC) over an inter-metal dielectric (IMD) layer, [2] forming via openings, [3] substantially conformally depositing a second ARC layer over the IMD layer and the via openings to cover the via opening sidewalls without filling the via openings, then [4] patterning an overlying photoresist layer with trench openings.

The Examiner disagrees. Lin's Figure 2a shows providing a thin conformal etch stop layer 120 over a lower layer dielectric (LLD) 110 (pointed out as an intermetal dielectric, IMD, when coated on metal, column 4 lines 55-61). Lin's etch stop layer 120 is disclosed to be silicon oxynitride (SiON, SiO_xN_y), silicon nitride (Si_3N_4, SiN), or titanium nitride (TiN) (e.g., to a

thickness of 500-1,500 Å, etc., column 5 lines 10-20). Lin's suitable ARC materials include titanium nitride (TiN), silicon oxynitride (SiON), and/or organic materials (column 5 lines 35-61). Lin recognized that the etch stop layer 120 would also possess ARC properties, at least when formed of either TiN or SiON. Therefore, Lin teaches [1] providing a first anti-reflectance coating (ARC) over an inter-metal dielectric (IMD) layer. After forming an upper layer dielectric (ULD), Lin teaches patterning a photoresist 145 having an opening 145′, as shown in Figure 2a and described at column 4 line 55 to column 5 line 24. A via opening 145 is etched through both dielectric layers and the intervening etch-stop layer (e.g., of ARC material, etc.) down to the substrate using the photoresist as an etching mask, then the photoresist is removed by oxygen ashing as shown in Figure 2b (column 5 lines 24-34). Even though described and shown in terms of a single via opening and overlapping trench, Lin's column 1 lines 22-31 clearly state the intention of forming plural grooves or trenches and conductive holes or via openings to form plural multi-level interconnects by repeating the dual damascene process as many times as is required. This encompasses formation of plural substantially adjacent via openings. Therefore, Lin also teaches subsequently [2] forming via openings. A main feature and key aspect of Lin's process includes formation of an anti-reflectance coating (e.g., ARC, bottom ARC (BARC), etc.) 150 as a protective cover over the dielectric (e.g., IMD, etc.) upper surface and in the via opening 145, covering the via sidewalls and bottom to the point of filling the via opening; then forming and patterning another photoresist layer 160 with an opening or trench 165′ over the via opening as shown in Figure 2c (column 5 lines 35-61). However, Yu and Filipiak have made obvious the formation of single or plural ARC layers that are only as thick as needed (specifically taught by Filipiak at column 3 lines 48-55), reducing a second ARC

layer thickness down to a thin conformal layer having a thickness of 50-1,500 Å. This suggests that ARC material could be saved and subsequent removal could even be avoided in Lin's dual damascene process by keeping the ARC layer(s) as thin as possible, while still preventing undesirable back scattering of light that leads to reflective notching of an overlying resist during patterning. Thus, the combined teachings of Lin, Yu, and Filipiak would motivate one of ordinary skill in the art to form Lin's ARC layer 150 by [3] substantially conformally depositing a second ARC layer over the IMD layer and the via openings to cover the via opening sidewalls without filling the via openings. Lin then also teaches [4] patterning an overlying photoresist layer with trench openings and etching the dielectric layer through the patterned photoresist (as shown in Figures 2d-2e and described at column 5 line 62 to column 6 line 7).

On pages 22-23, Appellants argue piecemeal analysis of each reference, Lin, Yu, and then Filipiak to support their contention that the combination of these references does not amount to a prima facie case of obviousness.

In response to Appellants' arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The basis for combining Lin, Yu, and Filipiak and the resulting combination of teachings taken together have been reiterated throughout prosecution and have again been set forth above.

Issue 5: Whether or not claims 15, 17, and 24 are unpatentable over Lin et al. (US Patent 6,042,999) in view of Yu et al. (US Patent 6,027,861), and further in view of Filipiak et al. (US Patent 5,918,147).

On page 24, Appellants reiterate their previous statements with respect to Issues 1, 2 and 4. Responses to these statements have already been set forth above.

Appellants again argue on page 24 that none of the cited references teach or suggest depositing a second ARC layer over an IMD layer and the via openings to cover the via opening sidewalls without filling the via openings.

The Examiner disagrees. Just as set forth above under Issue 4, a main feature and key aspect of Lin's process includes formation of an anti-reflectance coating (e.g., ARC, bottom ARC (BARC), etc.) 150 as a protective cover over the dielectric (e.g., IMD, etc.) upper surface and in the via opening 145, covering the via sidewalls and bottom to the point of filling the via opening; then forming and patterning another photoresist layer 160 with an opening or trench 165′ over the via opening as shown in Figure 2c (column 5 lines 35-61). However, Yu and Filipiak have made obvious the formation of single or plural ARC layers that are only as thick as needed (specifically taught by Filipiak at column 3 lines 48-55), reducing a second ARC layer thickness down to a thin conformal layer having a thickness of 50-1,500 Å. This suggests that ARC material could be saved and subsequent removal could even be avoided in Lin's dual damascene process by keeping the ARC layer(s) as thin as possible, while still preventing undesirable back scattering of light that leads to reflective notching of an overlying resist during patterning. Thus, the combined teachings of Lin, Yu, and Filipiak would motivate one of ordinary skill in the art to form Lin's ARC layer 150 by substantially conformally depositing a

second ARC layer over the IMD layer and the via openings to cover the via opening sidewalls without filling the via openings.

Also on page 24, Appellants assert that none of the references discloses the materials or range of thicknesses for the second ARC found in claims 15, 17, and 24. Claim 15 recites that [5] the second ARC is selected from the group consisting of silicon oxynitride and titanium nitride. Claim 17 recites that [6] the second ARC is formed within a range of thickness from about 100-1000 Å. Claim 24 recites that [7] the first and second ARCs consist essentially of silicon oxynitride.

The Examiner disagrees. Lin's suitable materials for ARC layer 150 include titanium nitride (TiN), silicon oxynitride (SiON), and/or organic materials (column 5 lines 35-61). Yu shows suitability of a TiN barrier layer as a thin conformal ARC layer (about 200-1,500 Å thick, shown as 18 in Figures 4-6 and as 46 in Figures 8-12, column 4 lines 33-62 and column 5 lines 27-37). Filipiak discloses tailoring plural ARC (e.g., silicon nitride, silicon-rich silicon nitride, silicon oxynitride, titanium nitride, etc.) layer combinations to their intended placement in a semiconductor device to avoid reflective notching when patterning an overlying photoresist layer (column 1 lines 11-20). Therefore, the combination of Lin, Yu, and Filipiak reads on a dual damascene process in which [5] the second ARC is selected from the group consisting of silicon oxynitride and titanium nitride and in which [7] the first and second ARCs consist essentially of silicon oxynitride. Filipiak's plural layer antireflective coatings (ARC) disclosed as suitable for semiconductor device manufacture include ARC 38 in Figure 5 which is composed of portions 380, 382, and 384 (column 3 lines 20-27) and conformal ARC 86 in Figure 10 which is composed of portions 861, 862, and 863 (column 4 lines 36-51). As shown in Figure 6 and

described at column 3 lines 48-55, ARC portions 380, 382, and 384 are 50, 100 and 200 Å thick, respectively, and are typically only as thick as needed to serve their intended purpose. Therefore, the combination of Lin, Yu, and Filipiak also reads on a dual damascene process in which an additional or second ARC is formed to be in the range of 50-1,500 Å thick, fully encompassing Appellants' recitation that [6] the second ARC is formed within a range of thickness from about 100-1000 Å.

Issue 6: Whether or not claim 18 is unpatentable over Lin et al. (US Patent 6,042,999) in view of Yu et al. (US Patent 6,027,861), and further in view of Filipiak et al. (US Patent 5,918,147).

On page 24, Appellants reiterate their previous statements with respect to Issues 1, 3 and 4. Responses to these statements have already been set forth above.

Issue 7: Whether or not claim 20 is unpatentable over Lin et al. (US Patent 6,042,999) in view of Yu et al. (US Patent 6,027,861), and further in view of Filipiak et al. (US Patent 5,918,147).

On page 25, Appellants reiterate their previous statements with respect to Issues 1 and 4. Responses to these statements have already been set forth above.

Appellants further argue on pages 25-26 that none of the references cited, alone or in combination, teach [8] forming a first ARC layer over first and second dielectric layers prior to forming a via opening and [9] substantially conformally depositing one additional ARC layer

over the IMD layer and the via openings to cover the via opening sidewalls without filling the via openings.

As stated above, Lin teaches a robust dual damascene photolithographic process with reduced light reflectance. The process starts by providing a semiconductor substrate having substructure devices formed in or on the substrate, including metal layers (column 4, lines 35-54). A lower layer dielectric (LLD) 110 (pointed out as an intermetal dielectric, IMD, when coated on metal, column 4 lines 57-61), a thin conformal etch-stop layer 120, and an upper layer dielectric (ULD) 130 are formed on the substrate. Both lower and upper dielectric (LLD and ULD) layers may be formed of silicon oxynitride (SiON, SiO_xN_y), silicon nitride (Si_3N_4, SiN), or silicon oxide by PECVD, CVD, PVD, or sputtering, preferably to a thickness of 8,000 to 15,000 Angstroms (Å) (column 5 lines 1-9). The etch-stop layer can be silicon oxynitride (SiON, SiO_xN_y), silicon nitride (Si_3N_4, SiN), or titanium nitride (TiN) (e.g., to a thickness of 500-1,500 Å, etc., column 5 lines 10-20). These layers are followed by forming and patterning a photoresist 145 having an opening 145′, as shown in Figure 2a and described at column 4 line 55 to column 5 line 24. Even though described and shown in terms of a single via opening and overlapping trench, column 1 lines 22-31 clearly state the intention of forming plural grooves or trenches and conductive holes or via openings to form plural multi-level interconnects by repeating the dual damascene process as many times as is required. This encompasses formation of plural substantially adjacent via openings. A via opening 145 is etched through both dielectric layers and the intervening etch-stop layer (e.g., of ARC material, etc.) down to the substrate using the photoresist as an etching mask, then the photoresist is removed by oxygen ashing as shown in Figure 2b (column 5 lines 24-34).

Lin's intervening placement of the etch stop layer (e.g., of ARC material, etc. placed between the upper and lower dielectric layers) protects the lower dielectric layer from undesirable over etching during subsequent etching of the upper dielectric layer to form an overlying trench. However, the etch stop layer (e.g., of ARC material, etc.) in this intervening position does not (a) provide ARC protection during patterning of the via resist 140 (as shown in Figure 2a) nor (b) prevent undesirable over etching of the upper dielectric 130 during etching of the via hole 145 (as shown in Figure 2b). In order to solve these problems, one of ordinary skill in the art would have noticed that Lin's etch stop material is also suitable for an ARC, at least when made of TiN or SiON (column 5 lines 35-61). So, one of ordinary skill in the art would have expected an additional layer of TiN or SiON etch stop/ARC material on top of the upper dielectric 130 before patterning of via resist 140 (as shown in Figure 2a) to (a) provide ARC protection during patterning of the via resist 140 in the same manner that an ARC 150 of TiN or SiON protects the trench resist 160 (as shown in Figure 2c) during patterning. Similarly, this additional layer of TiN or SiON etch stop/ARC material on top of the upper dielectric 130 before patterning of via resist 140 (as shown in Figure 2a) would also be expected to (b) prevent undesirable over etching of the upper dielectric 130 during etching of the via hole 145 (as shown in Figure 2b) in the same manner that etch stop layer 120 protects the lower dielectric 110 during subsequent trench etching (as shown in Figure 2e). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made in the combination dual damascene process taught by Lin, Yu, and Filipiak to have included an additional step of [8] forming a first ARC layer over first and second dielectric layers prior to forming a via opening, in order to (a) provide ARC protection during patterning of Lin's via resist 140 (as shown in Figure 2a) to

avoid reflective notching caused by back scattering and (b) prevent undesirable over etching of Lin's upper dielectric 130 during etching of the via hole 145 (as shown in Figure 2b).

As discussed above, a main feature and key aspect of Lin's process includes formation of an anti-reflectance coating (e.g., ARC, bottom ARC (BARC), etc.) 150 as a protective cover over the dielectric (e.g., IMD, etc.) upper surface and in the via opening 145, covering the via sidewalls and bottom to the point of filling the via opening; then forming and patterning another photoresist layer 160 with an opening or trench 165′ over the via opening as shown in Figure 2c (column 5 lines 35-61). However, Yu and Filipiak have made obvious the formation of single or plural ARC layers that are only as thick as needed (specifically taught by Filipiak at column 3 lines 48-55), reducing a second ARC layer thickness down to a thin conformal layer having a thickness of 50-1,500 Å. This suggests that ARC material could be saved and subsequent removal could even be avoided in Lin's dual damascene process by keeping the ARC layer(s) as thin as possible, while still preventing undesirable back scattering of light that leads to reflective notching of an overlying resist during patterning. Thus, the combined teachings of Lin, Yu, and Filipiak would motivate one of ordinary skill in the art to form Lin's ARC layer 150 by [9] substantially conformally depositing one additional ARC layer over the IMD layer and the via openings to cover the via opening sidewalls without filling the via openings.

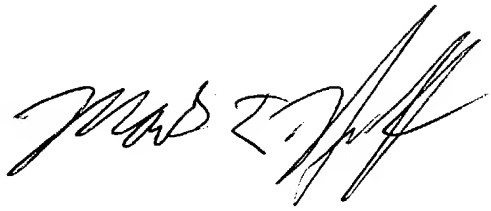
Conclusion

In their conclusion on pages 26-27, Appellants repeat their assertion of nonobviousness based on their step of covering via opening sidewalls by an ARC layer without filling the via

openings to solve the problem of light reflections from via opening sidewalls that cause undercutting of a resist layer in a trench patterning process.

Responses to this assertion have already been set forth above, especially under Issues 1-3, Issue 4 item [3], Issue 5, and Issue 7 item [9]. Lin points out that in a dual damascene process it is conventionally known to use a thin conformal etch barrier layer 50 of about 1,000 Å thick to cover the sidewalls of a hole through insulating layers, without filling the hole (see prior art Figures 1c-1f). Conventional etch barrier layer materials include silicon oxynitride (SiON, SiO_xN_y), silicon nitride (Si_3N_4, SiN) and/or titanium nitride (TiN) (column 2, lines 4-64). These same materials have also been shown useful for ARC layers, as noted above. In addition, Yu and Filipiak expand this range for ARC layer thickness to 50-1,500 Å, as previously explained. This establishes that coating (via) opening sidewalls with an ARC or etch barrier layer without filling the opening was within the level of ordinary skill at the time the invention was made. In fact, Filipiak teaches that an ARC layer is typically only as thick as needed, which suggests that ARC material could be saved and subsequent removal could even be avoided by keeping the ARC layer(s) as thin as possible, while still preventing undesirable back scattering of light that leads to reflective notching of an overlying resist during patterning. Therefore, Appellants' invention recited in claims 1-3, 7-8, 10-11, 13-15, and 17-24 as further argued in Appellants' brief is still held to be obvious over the combination of cited prior art by Lin, Yu, and Filipiak.

For the above reasons, it is believed that the rejections should be sustained.



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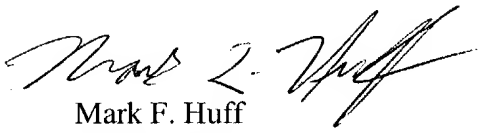
Respectfully submitted,

John Ruggles
Examiner
Art Unit 1756

jsr
December 22, 2004

Conferees:



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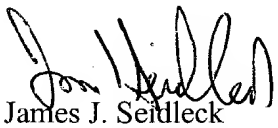

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